# COMPUTER ORGANIZATION

## COURSE OBJECTIVE:

The course is intended to provide student, the fundamentals of computer architecture (attributes of a multilevel machine, a system visible to Micro-architecture, Micro-Programming level) and organization (the operational components and their interconnections in the system), and the factors influencing the design of hardware and software elements to computer systems. Moreover, some advanced architectures will be presented.

**JNTU SYLLABUS:**

**UNIT I:**
**BASIC STRUCTURE OF COMPUTERS**: Computer Types, Functional unit, Basic OPERATIONAL concepts, Bus structures, Software, Performance, multiprocessors and multi computers. Data Representation. Fixed Point Representation. Floating – Point Representation. Error Detection codes.

**UNIT II:**
**REGISTER TRANSFER LANGUAGE AND MICROOPERATIONS**: Register Transfer language. Register Transfer Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit. Instruction codes. Computer Registers Computer instructions– Instruction cycle.
**Memory –** Reference Instructions. Input – Output and Interrupt. STACK organization. Instruction formats. Addressing modes. DATA Transfer and manipulation. Program control. Reduced Instruction set computer.

**UNIT III:**
**MICRO PROGRAMMED CONTROL:** Control memory, Address sequencing, micro program example, design of control unit Hard wired control. Micro programmed control

**UNIT IV:**
**COMPUTER ARITHMETIC:** Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit Decimal Arithmetic operations.

**UNIT V**
**THE MEMORY SYSTEM:** Basic concepts semiconductor RAM memories. Read-only memories Cache memories performance considerations, Virtual memories secondary storage. Introduction to RAID.

**UNIT-VI:**
**INPUT-OUTPUT ORGANIZATION:** Peripheral Devices, Input-Output Interface, Asynchronous data transfer Modes of Transfer, Priority Interrupt Direct memory Access, Input –Output Processor (IOP) Serial communication; Introduction to peripheral component, Interconnect (PCI) bus. Introduction to standard serial communication protocols like RS232, USB, and IEEE1394.

**UNIT VII:**
**PIPELINE AND VECTOR PROCESSING:** Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline Vector Processing, Array Processors.

**UNIT VIII:**
**MULTI PROCESSORS:** Characteristics or Multiprocessors, Interconnection Structures, Interprocessor Arbitration. InterProcessor Communication and Synchronization Cache Coherence. Shared Memory Multiprocessors.

**SUGGESTED BOOKS**

**TEXT BOOKS:**

**T1:** Hamacher, Vranesic, Zaky, ***'Computer Organization'*** - V Edition.McGraw Hill.

**T2:** Morris Mano , ***'Computer System Architecture'*** - III Edition.PHI/Pearson.

**REFERENCE BOOKS:**

**R1:** Stallings William, ***'ComputerOrganization & Architecture'*** - VI Edition.PHI/Pearson

**R2:** Tanenbaum Andrew S, ***'Structured computer Organization'*** -IV Edition.PHI/Pearson

**R3:** Sivaraama Dandamudi Springer, ***'Fundamentals of Computer Organization and Design'*** -Int.Edition.

**R4:** John L. Hennessy and David A. Patterson, ***'Computer Architecture a quantitative Approach'*** -4th Edition Elsevier

**R5:** Joseph D. Dumas II, ***'Computer Architecture: Fundamentals and Principles of Computer Design'*** –BS Publication.

# Session Plan

| Topics in each unit as per JNTU syllabus | Lecture No. | Modules/Sub-modules for each Topic | Text Books/ Reference Books |
|---|---|---|---|
| | **1** | **Introduction:**<br>**Objective:** Is to understand the Structure of Basic Computer, and Modular Organization of Components like, CPU, Bus, I/O, and Memory. Also we are going to study the increase of performance by introducing RAID, Parallel Processing by Pipelining in Uniprocessor systems, at the end we are going to study some complex systems which support Multiprocessors and their structural organizations. | |
| **BASIC STRUCTURE OF COMPUTERS**:<br>Computer Types | **2** | **Basic structure of Computers:**<br>Generation of Computers, Machines with Generations, Von Neumann architecture, Performance Issues, Classification of computers.<br>**Types of Computer**<br>Mini, Super, Personal, notebook, Main Frame, workstation computer etc. | T1:1.1<br>R1:Pg 16-36 |
| Functional unit,<br>Basic operational concepts, | **3** | **Block Diagram of Computer:**<br>Central Processing Unit, Control Unit, Memory, Arithmetic Logical unit, Set of Internal Registers, System Bus, I/O Module, Input/Output Devises | T1:1.2,1.3<br>R1:Pg 50-58 |

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|---|---|---|---|
| | | **Basic Operational Concepts:**<br>Instruction Execution, Memory Fetch | |
| Bus structures, | **4** | **Bus Structures:**<br>Multiple—bus Hierarchies, Traditional Bus Architecture, High—Performance Architecture, PCI Bus | T1:1.4<br>R1:Pg 69-80 |
| Software,<br>Performance, | **5** | **Software:**<br>Operating System, System Software's, Application Software's, and End user Software's.<br>**Performance:**<br>Speed, Response Time, Throughput, Access Time. | T1: 1.5,1.6 |
| Multiprocessors and multi computers.<br>Data Representation. | **6** | **Multiprocessors and Multicomputers**<br>**Data Representation**<br>Number System, Complements(1's and 2's) | T2: 3.1,3.2<br>T1:1.7 |
| Fixed Point Representation. Floating Point Representation. | **7** | **Fixed Point Representation**<br>Signed Magnitude Representation, 1s Complement Representation, 2s Complement Representation, Decimal Fixed Point Representation<br>**Floating Point Representation** | T2 :3.3,3.4 |
| Error Detection codes. | **8** | Grey Code, Excess-3 Code, weighted codes, self complement codes.<br>**Error Detection Codes**<br>Parity, Hamming Code. | T2: 3.5,3.6 |
| | **9** | Tutorial: Unit-I | |
| | **10** | Revision: Unit-I | |
| | | **UNIT-II** | |
| **REGISTER TRANSFER LANGUAGE AND MICROOPERATIONS**:<br>Register Transfer language. Register Transfer Bus and memory transfers | **11** | **Register Transfer Language and Micro operations:**<br>**Register Transfers**<br>**Bus** Lines, Multiplexed Bus Lines, Three State Buffer Bus Lines<br>**Memory Transfer**<br>Read, Write | T2:4.1-4.3 |
| Arithmetic Micro operations | **12** | **Arithmetic Micro operations:**<br>Adder→Half and Full Adder, Adder-Subtractor, Binary Incrementor, Arithmetic Circuit | T2:4.4 |
| logic micro operations,<br>shift micro operations,<br>Arithmetic logic shift unit | **13** | **Logic Microoperations:**<br>Logic Circuit, Applications<br>**Shift Microoperations**<br>Logical Shift Operation<br>**Arithmetic Logic Shift Unit**<br>Arithmetic logic shift Circuit | T2:4.5-4.7 |
| Instruction codes,<br>Computer Registers,<br>Computer instructions. | **14** | **Instruction codes**<br>**Computer Registers**<br>PC, AR, IR, TR, DR, AC, OUTR, INPR, Connection of Registers with Common bus.<br>**Computer Instruction**<br>Instruction Format of Basic Computer, Basic Computer Instructions | T2:5.1-5.3 |
| Instruction cycle | **15** | Control Unit of Basic Computer, Timing of Signals.<br>**Instruction Cycle:**<br>Fetch, Decode, Execute Cycle, Indirect Fetch | T2:5.4,5.5 |
| **Memory – Reference Instructions**,<br>Input – Output | **16** | **References Instruction**<br>Register Reference Instruction, Memory Reference Instruction, I/O Reference Instruction | T2: 5.5-5.7 |
| Interrupt | **17** | **Interrupts:**<br>Interrupt Cycle | T2: 5.7 |

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|---|---|---|---|
| STACK organization | **18** | **Stack Organization**<br>Register Stack, Memory Stack, Evolution of Arithmetic Expression | T2: 8.3 |
| Instruction formats | **19** | **Instruction Formats**<br>Zero, One, Two and Three address instructions | T2: 8.4<br>R2:11.3 |
| Addressing modes | **20** | **Addressing Modes**<br>Immediate, Direct, Indirect, Register Direct, Register Indirect, Displacement, Stack. | T2:8.5<br>R2:11.1 |
| DATA Transfer and manipulation,<br>Program control. | **21** | **Data Transfer and Manipulation:**<br>**Data Transfer**<br>Data **Manipulation,** Arithmetic, Logical and bit manipulations, Shift Instructions<br>**Control Instructions**<br>Interrupts, External, Internal, Software | T2:8.6,8.7 |
| Reduced Instruction set computer | **22** | **RISC( Reduced Instruction Set Computers)** | T2: 8.8<br>R2:13.1,13.4,13.8 |
| | **23** | Tutorial: Unit-II | |
| | **24** | Revision: Unit-II | |
| | | **UNIT-III** | |
| **MICRO PROGRAMMED CONTROL:**<br>Control memory | **25** | **Micro Programmed Control:**<br>Micro Operations<br>**Control memory** | T2:ch7.1<br>R1:ch17.1 |
| Address sequencing | **26** | Micro Instruction formats<br>Horizontal Micro instructions, Vertical Micro instructions<br>**Address Sequencing** | T2:ch7.2,7.3<br>R1:ch17.1,17.2 |
| micro program example | **27** | **Microinstruction execution**<br>Vertical/horizontal, Packed/unpacked, Hard/soft microprogramming, Direct/indirect encoding | T2:ch7.3<br>R1:ch17.3 |
| Design of control unit Hardwired control. Microprogrammed control | **28** | **Design of control unit**<br>**H/Wired Control Unit Design, Micro programmed Control** | T2:ch7.4<br>R1:ch16.3 |
| | **29** | Tutorial: Unit-III | |
| | **30** | Revision: Unit-III | |
| | | **UNIT-IV** | |
| **COMPUTER ARITHMETIC:**<br>Addition and subtraction | **31** | **Computer Arithmetic, Fixed Point arithmetic**<br>**Addition, Subtraction,** H/W implementations | T2:ch10.2 |
| multiplication Algorithms | **32** | **Multiplication**<br>Booths Algorithm, Array multiplier, H/W implementations | T2:ch10.3<br>R1:ch9.3 |
| Division Algorithms, Floating – point Arithmetic operations | **33** | **Division:** H/W implementation<br>**Floating Point arithmetic:**<br>Addition, Subtraction, H/W implementations | T2:ch10.4,10.5<br>R1:ch9.3 |
| Multiplication, Division,<br>H/W implementations | **34** | **Multiplication, Division,**<br>H/W implementations | T2:ch10.5<br>R1:ch9.4, |
| Decimal Arithmetic unit<br>Decimal Arithmetic operations | **35** | **Decimal Arithmetic unit,**<br>**Decimal Arithmetic operation** | |
| | **36** | Tutorial: Unit-IV | |
| | **37** | Revision: Unit-IV | |
| | | **UNIT-V** | |
| **THE MEMORY SYSTEM:** | **38** | **The Memory System;** Block Diagram of Memory Unit, Hierarchy of Memory Unit, Characteristics of Memory | T2:ch12.1<br>R1:ch4.1 |
| Basic concepts semiconductor RAM memories | **39** | **Physical View of the memory, Semiconductor Memory,** Static and Dynamic Memory, Synchronous and Asynchronous Memory | R1:ch5.1 |
| Read-only memories | **40** | **Mapping of Memory Address, Associative Memory** | T2:12.2,12.3 |
| | **41** | **H/W implementation of Associative Memory** | T2:12.3 |
| Cache memories performance | **42** | **Cache memory: Memory Mappings:** Direct Mapping, | T2:12.5 |

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|---|---|---|---|
| considerations | | Associative Mapping, Set Associative Mapping | R1:ch4.3 |
| secondary storage | **43** | **Auxiliary Memory:** Magnetic Tape, Magnetic Disk, Optical Disk | R1:ch6.1,6.3 ,6.4 |
| Virtual memories | **44** | **Virtual Memory:** Paging, Segmentation | T2:ch12.7 |
| Introduction to RAID | **45** | **RAID:** Adv and Dis-Adv, RAID Levels(0-6) | R1:ch6.2 |
| | **46** | Tutorial: UnitI V | |
| | **47** | Revision: Unit-V | |
| **UNIT-VI** | | | |
| **INPUT-OUTPUT ORGANIZATION:** Peripheral Devices | **48** | **Input—Output Organization** **Peripheral devices,** Mouse, keyboard, monitor etc., ASCII alpha numeric characters | T2:ch11.1 |
| Input-Output Interface | **49** | **Input-Output Interface,** I/O Bus and Interface modules, I/O versus Memory, Isolated versus memory mapped I/O | T2:ch11.2 |
| Asynchronous data transfer | **50** | **Asynchronous Data Transfer,** Strobe Control, Handshaking, Asynchronous communication interface, Asynchronous Serial Transfer, FIFO Buffer. | T2:ch11.3 |
| Modes of Transfer | **51** | **Modes of Transfer,** Programmed I/O, Interrupted I/O, DMA. | T2:ch11.4 |
| Direct memory Access | **52** | **Direct Memory Access**, DMA controller, DMA transfer | T2:ch11.6 |
| Priority Interrupt | **53** | **Priority Interrupt,** Daisy-chaining priority, Parallel priority interrupt, Priority encoder, Interrupt cycle, software routines, Initial and final operations | T2:ch11.5 |
| Input –Output Processor (IOP) | **54** | **I/O Processor,** CPU-IOP communication, IBM 370/I/O channel Intel 8089 IOP | T2:ch11.7 |
| Serial communication | **55** | **Serial Communication,** Character-oriented protocol, Data transparency, Bit-oriented Protocol | T2:ch11.8 |
| Introduction to peripheral component. Interconnect (PCI) bus. Introduction to standard serial communication protocols like RS232, USB, and IEEE1394 | **56** | **Standard I/O Interfaces,** Peripheral Component Interconnect(PCI) Bus, Universal Serial Bus(USB), Lecture Material for RS232, IEEE1394 | T1:ch4.7 LM |
| | **57** | Tutorial: UnitI VI | |
| | **58** | Revision: Unit-VI | |
| **UNIT-VII** | | | |
| **PIPELINE AND VECTOR PROCESSING:** Parallel Processing, | **59** | **Pipeline and Vector Processing,** Flynn's Classification, **Parallel Processing,** Pipe lining, Vector Processing, Array Processor | T2:ch9.1,9.2 |
| Pipelining, Arithmetic Pipeline | **60** | **Pipelining,** Arithmetic Pipelining | T2:ch9.3 |
| Instruction Pipeline RISC Pipeline | **61** | Instruction Pipelining, RISC Pipelining | T2:ch9.4,9.5 |
| RISC Pipeline Vector Processing, Array Processors | **62** | **Vector Processing,** Memory interleaving, **Array Processor** Attached Array Processor, SIMD Array Processor | T2:ch9.6,9.7 |
| | **63** | Tutorial: UnitI VII | |
| | **64** | Revision: Unit-VII | |
| **UNIT-VIII** | | | |
| **MULTI PROCESSORS:** Characteristics or Multiprocessors | **65** | **Multi Proce66ssors, Characteristics of multiprocessors,** Load Sharing, Reliability, Tightly and Loosely Coupled | T2:ch13.1 |
| Interconnection Structures | **66** | **Interconnection Structures:** Time-shared common Bus, Multi port memory, Cross bar switch, Multi stage switching network hypercube interconnection | T2:ch13.2 |
| Interprocessor Arbitration | **67** | **Interprocessor Arbitration,** Serial arbitration procedure, Parallel arbitration logic, Dynamic arbitration algorithms. | T2:ch13.3 |
| Inter Processor Communication | **68** | **Inter processor communication and synchronization,** Master Slave Configuration, Separate Operating System, Distributed Operating System | T2:ch13.4 |

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| Synchronization | **69** | Inter processor Synchronization, Mutual exclusion with a semaphore | T2:ch13.4 |
| Cache Coherence | **70** | **Cache Coherence,** Solutions to cache coherence problem | T2:ch13.5 |
| Shared Memory Multiprocessors | **71** | Shared Memory Multiprocessor, UMA, NUMA | R3:ch1 |
| | **72** | Tutorial: UnitI VIII | |
| | **73** | Revision: Unit-VIII | |

## BOOKS REFERED BY FACULTY:

### TEXT BOOKS:

**T1:** Hamacher, Vranesic, Zaky, ***'Computer Organization'*** - V Edition.McGraw Hill.

**T2:** Morris Mano , ***'Computer System Architecture'*** - III Edition.PHI/Pearson.

### REFERENCE BOOKS:

**R1:** Stallings William, ***'ComputerOrganization & Architecture'*** - VI Edition.PHI/Pearson

**R2:** Tanenbaum Andrew S, ***'Structured computer Organization'*** -IV Edition.PHI/Pearson

**R3:** Sivaraama Dandamudi Springer, ***'Fundamentals or Computer Organization and Design'*** -Int.Edition.

**WEBSITES :**

| S.No. | Description/topic/University | Website |
|---|---|---|
| 1 | **Complete tutorial on Computer Organization by William stallings Covers all topics** | http://williamstallings.com/COA5e.html |
| 2 | **Wayne State University. Covers the topic; memory, pipelining, I/O.** | http://www.ece.eng.wayne.edu/~gchen/ece4680/lecture-notes/lecture-notes.html |
| 3 | **University of Maryland Covers all topics** | http://www.cs.umd.edu/class/sum2003/cmsc311/Notes/ |
| 4 | **Korea University of Technology and education Covers all topics** | http://microcom.kut.ac.kr/labs/labs_comarc_menu.htm |
| 5 | **University of Massachusetts Amherst Covers RAID** | http://www.ecs.umass.edu/ece/koren/architecture/Raid/raidhome.html |
| 6 | **University of Wisconsin-Madison** | http://www.ece.wisc.edu/~mikko/352/Chapter-7-sli6.pdf |

**JOURNALS:**

| S.No. | Journal | Web site |
|---|---|---|
| 1. | Journal of System Architecture | **http://www.elsevier.com/wps/find/journaldescription.cws_home/505616/description#description** |
| 2. | Journal of Parallel and Distributed Computing | **http://www.informatik.uni-trier.de/~ley/db/journals/jpdc/** |
| 3. | Jnl of Microcomputer Applications | **http://www.ingentaconnect.com/content/ap/mx** |
| 4. | The Journal of Super Computing | **http://springerlink.metapress.com/content/100302/** |
| 5. | ACM Trans on Computer Systems | **http://www.acm.org/pubs/journals.html** |
| 6. | Standards and Interface Journal | **http://www.elsevier.com/wps/find/journaldescription.cws_home/505607/description#description** |
| 7. | Microprocessing and Microprogramming | **http://journalseek.net/cgi-bin/journalseek/journalsearch.cgi?field=issn&query=0165-6074** |
| 8. | IEEE Journal on Computer Architectures for Intelligent Machines | **http://www2.computer.org/portal/web/csdl/doi/10.1109/MC.1992.10044** |

**STUDENT SEMINAR TOPICS:**

| S.No. | Topics | References |
|---|---|---|
| 1. | **Architecture of PDP-8.** | **http://userpages.wittenberg.edu/bshelburne/Comp255S/PDP8n01.htm** |
| 2. | **Architecture of PDP-11** | **http://portal.acm.org/citation.cfm?id=1067629.806527** |
| 3. | **Architecture of IBM 360.** | www.research.**ibm**.com/journal/rd/082/**ibm**rd0802C.pdf |
| 4. | **Architecture of CRAY-I** | http://archive.computerhistory.org/resources/text/Cray/Cray.EASeries.1988.102646184.pdf |
| 5. | **RS6000** | **http://www-ugrad.cs.colorado.edu/~csci4576/RS6000/RS6000.html** |
| 6. | **RISC Processor** | **http://6004.csail.mit.edu/Fall97/L28.pdf** |
| 7. | **Architectures of 8085, 8086 and Pentium** | **Text book: Ramesh S Gaonkar, Douglas V Hall.**<br>http://pages.cs.wisc.edu/~smoler/x86text/lect.notes/Pentium.html |
| 8. | **Architecture of Array Processor AP120B** | www.arubanetworks.com/pdf/products/DS_**AP120**-121.pdf |

**ASSIGNMENT QUESTIONS :**

**UNIT-I**

1. Explain different types of computers.
2. Explain functional units in computer.
3. Explain connections between the processor and memory.
4. What is the difference between single bus structure and multiple bus structure.
5. What is the difference between multiprocessor and multi computers.
6. Write notes on number systems.
7. Explain the conversion of decimal to binary numbers.
8. Explain how to perform subtraction of unsigned numbers.
9. Write notes on fixed point representation.
10. Explain 3 possible ways of integer representation.
11. Explain 2's compliment Arithmetic addition and subtraction.
12. Write notes on Decimal fixed point representation.
13. Write notes on 4bit gray code & decimal codes.
14. Explain weighted code & excess 3 code.
15. Write notes on Error detection codes.

**UNIT-II**

1. What is register transfer language.
2. What is register transfer & Give the block diagram of register.
3. Explain bus and memory transfer.
4. Write notes on three state bus buffers.
5. Explain Arithmetic micro operations.
6. Write notes on Binary adder & Binary Adder- Subtracter.
7. Explain 4 bit Arithmetic circuit.
8. Write notes on logic micro operations with hardware implementation.

9. Write notes on shift micro operations with hardware implementation.
10. Write notes on Arithmetic logic shift unit with hardware implementation.
11. What is an instruction code & Explain how the stored program organization is implemented.
12. What is Direct address & Indirect address ? Explain it?
13. What are basic computer registers. Mention and explain it.
14. Explain how Basic computer register connected to common bus.
15. Write notes on computer instructions.
16. What is an instruction cycle .Give the flow chart for instruction cycle.
17. Write notes on memory reference instructions.
18. Explain about stack organization.
19. Write notes on Reduced instruction set computer.
20. Write notes on data transfer & manipulation.

**UNIT-III**

1. What is control memory.
2. What is micro program & micro instruction.
3. Explain micro program control organization.
4. Write notes on pipeline register.
5. What is mapping process & Give the address sequencing capabilities required in a control memory.
6. Explain selection of address for control memory.
7. What is subroutines & Explain mapping of instructions.
8. Write notes on micro program.
9. Explain computer hardware configuration with neat diagram.
10. Explain micro instruction format.
11. What is conditional field & branch field.
12. Write notes on Symbolic micro instruction.
13. Write notes on Symbolic micro program.

14. Write notes on Binary micro program.
15. Explain fetch & decode phases.
16. Write notes on Design of control unit.
17. Write notes on micro program sequence.
18. Explain with neat diagram of micro program sequence for a control memory.
19. Explain hardwired control unit.
20. Explain micro programmed control unit.

**UNIT-IV**

1. What is an algorithm & explain signed magnitude representation.
2. Explain addition & subtraction with signed magnitude data.
3. Explain hardware implementation for signed magnitude data addition & subtraction.
4. Give the flowchart for add & subtract operations.
5. Explain addition and subtraction with signed 2's compliment data.
6. Write notes on multiplication algorithm with hardware implementation for signed magnitude data.
7. Give the hardware algorithm flowchart for multiply operation.
8. Explain BOOTH multiplication algorithm.
9. Give hardware BOOTHS algorithm for multiplication of signed 2's compliment numbers.
10. What is an array multiplier & explain 2-bit by 2-bit array multiplier.
11. Explain 4-bit by 3-bit array multiplier.
12. Explain division algorithm.
13. Write notes on hardware implementation of division algorithm for signed magnitude data.
14. Give the flowchart for divide operation.
15. Explain floating point arithmetic operation.
16. Give the flowchart for addition & subtraction of floating point numbers.
17. Give the flowchart for multiplication of floating point numbers

18. Give the flowchart for division of floating point numbers

19. Write notes on decimal arithmetic unit.

20. Write notes on decimal arithmetic operations.

**UNIT-V**

1. Write notes on basic concepts of semiconductor RAM memories.
2. Explain memory hierarchy in a computer system.
3. Differences between auxiliary memory & main memory.
4. Write notes on cache memory.
5. Difference between static RAM & dynamic RAM.
6. Difference between RAM & ROM.
7. What is bootstrap loader & write notes on RAM & ROM chips.
8. Write notes on memory connections to cpu.
9. Write notes on magnetic disks & magnetic tapes.
10. What is cache memory . give the mapping techniques of cache memory.
11. Write notes on Direct mapping technique.
12. Write notes on Associative mapping technique.
13. Write notes on set associative mapping technique.
14. Write notes on cache initialization.
15. Write notes on virtual memory.
16. Give memory table for mapping a virtual address.
17. Write notes on cache memories performance considerations.
18. Write notes on RAID.
19. Write notes on RAID levels.
20. Write notes on page replacement algorithm.

**UNIT –VI**

1. Write notes on peripheral devices.

2. Write notes on magnetic tapes & magnetic disks.
3. Explain input-output interface.
4. Difference between I/O bus & Interface modules.
5. Difference between I/O bus & memory bus.
6. Difference between Isolated and memory mapped I/O
7. Give an example of I/O interface.
8. Write notes on Asynchronous data transfer.
9. What is an hand shaking signal. Give its timing diagram.
10. Give the difference between Synchronous and Asynchronous transmission.
11. Give the circuit diagram for 4*4 FIFO buffer.
12. Write notes on modes of transfer.
13. What is DMA & Explain DMA in detail.
14. Write notes on programmed I/O.
15. Write notes on interrupt initiated I/O.
16. What is priority interrupt? Explain Daisy chaining priority.
17. Give the Block diagram of DMA controller.
18. What is cycle stealing& write notes on DMA transfer.
19. Write notes on IOP, PCI.
20. Write notes on standard serial communication protocols like RS-232,USB ,IEEE 1394.

**UNIT-VII**

1. What is parallel processing. And give the multiple functional units .
2. Write notes on Flynn's classification.
3. What is pipelining & give the example of pipeline.
4. Give neat diagram of Four-segment pipeline.
5. Write notes on Arithmetic pipeline.

6. Give flowchart for pipeline floating point addition & subtraction .
7. Write notes on instruction pipeline.
8. Give flowchart for four segment cpu instruction pipeline.
9. Write notes on hardware interlocks,operand forwarding, delayed load.
10. What is delayed branch & branch prediction.
11. Write notes on RISC pipeline.
12. Explain three segment instruction pipeline.
13. Write notes on vector processing & memory interleaving.
14. Explain super computers & vector operations.
15. Give the instruction format for vector processor.
16. Write notes on Array processor.
17. Write notes on Attached array processor.
18. Write notes on SIMD array processor with neat diagram.
19. Give an example that uses delayed load with three segment pipeline of RISC.
20. Write the difference between SISD & SIMD processor.

**UNIT-VIII**

1. Write notes on multiprocessor.
2. Give the characteristics of multiprocessor.
3. Give the difference between tightly coupled & loosely coupled.
4. Explain time shared common bus with neat diagram.
5. Write notes on multi port memory.
6. Distinguish between local memory and shared memory.
7. Give the block diagram of crossbar switch.
8. Write notes on multistage switching network.
9. Explain binarytree with 2X2 switches.
10. Write notes on 8X8 omega switching network.

11. Write notes on Hypercube interconnection.
12. Write the difference between synchronous & asynchronous bus.
13. Write notes on system bus.
14. Give neat diagram of serial (daisy chain) arbitration .
15. Give neat diagram of parallel arbitration .
16. Explain dynamic arbitration algorithms.
17. Write notes on polling, LRU, FIFO, rotating daisy chain.
18. Write notes on Interprocessor communication & synchronization.
19. How the cache coherence problem occurs.
20. Give the solutions to cache coherence problem.

**QUESTION BANK :**

**UNIT – I**

1. (a) What are the different performance measures used to represent a computer systems performance?
(b) Explain about Amdhal's Law. (may 2009)
2. (a) Explain the terms compiler, linker, assembler, loader and describe how a C program or any other high level language program is executed in a system. Indicate entire process with a figure.
(b) Distinguish between high level and low level languages?. What are the requirements for a good programming language? (JNTU Apr/May 2009)

3. (a) What are the different interconnection structures used in multiprocessors? Explain about multistage crossbar switch. [8]
(b) Support or oppose the statement ?Every efficient serial program is efficient parallel program? (JNTU Apr/May 2009)

4. (a) What are the different interconnection structures used in multiprocessors? Explain about multistage crossbar switch. [8]
(b) Support or oppose the statement ?Every efficient serial program is efficient parallel program? (JNTU Apr/May 2009)

5. Describe all optional PCI signal lines with designation and type. **(Sep 08, Feb 07)**

6. (a) Draw and explain the timing of read operation in both synchronous and asynchronous timing.
(b) Discuss various data transfer types supported by buses **(Sep 08)**

7. (a) Differentiate between traditional and high performance bus architectures
(b) List the key elements of bus design. **(Sep 08)**

8. Explain the generic structure of IAS computer in detail with the help of a block diagram. **(Sep 08, May 04)**

9. (a) Explain about IAS memory formats.
(b) List various registers in a computer along with their purpose **(May 08)**

10. (a) Explain the purpose and merits of interrupts.
(b) Draw and explain the instruction cycle with interrupts.
(c) What is interrupt handler? Explain its purpose. **(May 08)**

11. (a) Define PCI. Explain the applications of PCI
(b) Describe any ten mandatory PCI signals. **(May 08)**

12. (a) Discuss the interconnection structure design of a computer.
(b) Explain various bus lines.
(c) What do you mean by multiple - bus hierarchies **(May 08)**

13. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
(b) Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.

(c) Distinguish between tightly coupled microprocessors and tightly coupled Microprocessors. **(Feb 08)**

14. (a) Explain the terms computer architecture, computer organization and computer design in a detailed fashion.
    (b) Explain about MIPS, FLOPS rating of a processor. How do we arrive at these values. **(Feb 08)**

15. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.
    (b) Distinguish between high level and low level languages? What are the requirements for a good programming language? **(Feb 08)**

16. (a) Explain the top level view of components
    (b) What do you mean by hard wired program?
    (c) List the basic functions performed by a computer. **(Nov 07)**

17. Write an algorithm to find all allowable weights for a "weighted BCD code". Assume that all weights are positive numbers. **(Nov 07)**

18. Explain the expanded structure of IAS computer with a neat block diagram. **(Nov 07, May 04)**

19. (a) Explain about the arithmetic in excess - 3 code.
    (b) Discuss about normalized floating point representation. **(Nov 07)**
20. (a) What is instruction Cycle ?
    (b) Elaborate the characteristics of a hypothetical machine
    (c) What do you mean by hardwired program? **(Nov 07)**
21. (a) Find the output binary number after performing the following arithmetic operations
    i. 111.01 + 10.111
    ii. 11.01 + 110.11
    iii. 110.11 - 111.01
    (b) Explain about the longhand division of binary integers. **(Nov 07)**

22. Explain about error detecting and correcting codes. What is their relevance.

23. Difference between multiprocessors and multicomputers. **(Feb 07)**

24. Explain about Von Neumann architecture design in detail. **(Feb 07, Nov 06, May 04)**

25. i. Differentiate between dedicated and multipludged bus line
    ii. Discuss various methods of bus arbitration.
    iii. What do you mean by bus width? **(Feb 07)**

**UNIT – II**

1. There exists three 4-bit registers (A,B, and C) and 4-bit data lines (say D). Design a circuit to transfer data from any register to any other register including data lines and vice versa. (JNTU Apr/May 2009)

2. Design a circuit for parallel load operation into one of the four 4-bit registers from a bus. Mention clearly control/selection bits and selection logic. Assume RS flip-flops. (JNTU Apr/May 2009)

3. Design a circuit for parallel load operation into one of the four 4-bit registers from a bus. Mention clearly control/selection bits and selection logic. Assume JK flip-flops. (JNTU Apr/May 2009)

4. Design a circuit which can be used to transfer data from any register to any other register out of four 4-bit registers A,B,C,D which uses RS flip-flops. [16] (JNTU Apr/May 2009)

5. (a) Find the output binary number after performing the arithmatic operation using 1's complement representation.
   i. 111.01 + 10.111
   ii. 110.11 - 111.01
   (b) Explain steps involved in the addition of numbers using 2's complement notation **(Sep 08)**

6. (a) Explain about booth coding
   (b) Find the booth coded numbers of the following binary numbers
   i. 01101111101
   ii. 000111110110 **(Sep 08)**

7. Discuss about
   (a) Weighted codes
   (b) Self - complementing codes
   (c) Cyclic codes **(Sep 08)**

8. Write an algorithm to substract binary numbers represented in normalized floating point mode with base 2 for exponent **(Sep 08)**

9. (a) Find the output binary number after performing the following arithmetic operations
   i. 111.01 + 10.111
   ii. 11.01 + 110.11
   iii. 110.11 - 111.01
   (b) Explain about the longhand division of binary integers. **(May 08)**

10. (a) How subtraction is done on the binary numbers represented in one's complement notation give an examples.
   (b) What do you mean by r's complement. **(May 08)**

11. Write an algorithm to substract binary numbers represented in normalized floating point mode with base 2 for exponent **(May 08)**

12. (a) Find the output binary number after performing the arithmatic operation using 1's complement representation.
   i. 111.01 + 10.111
   ii. 110.11 - 111.01
   (b) Explain steps involved in the addition of numbers using 2's complement notation.
   **(May 08)**

13. (a) Explain about stack organization used in processors. What do you understand by register stack and memory stack?
   (b) Explain how X=(A+B)/(A-B) is evaluated in a stack based computer. **(Feb 08)**

14. (a) What is the use of buffers. Explain about tri-state buffers. Explain about high impedance state.
   (b) Explain commonly employed bit shift operators such as shift left, right, circular shift left/right and arithmetic shift left/right. Assume an 8-bit register, give an example for each
   **(Feb 08)**

15. Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. **(Feb 08)**

16. (a) Explain about user-visible registers.
    (b) Compare register organizations Z 8000 with 8086 processors. **(Feb 08)**

17. (a) Discuss the motivation for CISC.
    (b) Differentiate between CISC and RISC characteristics. **(Nov 07)**

18. Discuss about various Pentium addressing modes with algorithms. **(Nov 07)**

19. (a) Differentiate between large register file versus cache.
    (b) Discuss how compiler based register optimization is done.
    (c) Explain various characteristics of reduced instruction set architectures. **(Nov 07)**

20. List integer arithmetic, logical and shift operations of power PC with description. **(Nov 07)**

21. (a) List and describe integer arithmetic and logical instructions of Motorola 88000.
    (b) Discuss about functioning of Motorola 88000 instruction unit pipeline. **(Nov 07)**

22. i. Define element of machine instruction.
    ii. How various instructions are categorized?
    iii. Explain about simple instruction format **(Feb 07)**

23. Convert the following decimal numbers to base three to base five.
    i. 73
    ii. 10.333
    iii. 21.25 **(Feb 07)**

24. i. Explain how floating point division is done?
    ii. Explain the addition binary number in 1's Complement notation. **(Feb 07, Nov 06)**

25. i. Draw and explain the instruction cycle state diagram that includes interrupt cycle processing.
    ii. Discuss about transfer of control with multiple interrupts. **(Feb 07)**

**UNIT – III**

1. (a) How do we reduce number of microinstructions. What are micro-subroutines? [8]
(b) Explain nanoinstructions and nanometry. Why do we need them? [8] (JNTU Apr/May 2009)

2. (a) Support or oppose the statement. If we want to add a new machine language instruction to a processors instruction set, simply write a C program and compile and store the resultant code in control memory. [8]
(b) Why do we need subroutine register in a control unit? Explain. [8] (JNTU Apr/May 2009)

3. (a) What are the design goals for a designer while deciding a hardwired or micro-programmed CU for a CPU? [8]
(b) Explain nanoinstructions and nanometry. Why do we need them. [8] (JNTU Apr/May 2009)

4. (a) Differentiate between microprogramming and nanoprogramming. [8]
(b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [8] (JNTU Apr/May 2009)

5. (a) Explain various control and status registers.
   (b) Compare register organizations of 8086 with MC68000 processors **(Sep 08)**

6. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. **(Sep 08, May 08)**

7. (a) Discuss about power PC data types
   (b) Explain numerical data formats for Pentium floating point unit. **(Sep 08)**

8. (a) Describe various Pentium data types
   (b) Describe various common data transfer instruction set operations. (**May 08)**

9. Discuss about various Pentium addressing modes with algorithms (**May 08)**

10. (a) Support or oppose the statement. The control unit is a firmware?
    (b) Support or oppose the statement. If we want to add a new machine language instruction to a processors instruction set, simply write a C program and compile and store the resultant code in control memory. **(Feb 08)**

11. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction.
    (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. **(Feb 08)**
12. (a) Differentiate between microprogramming and nanoprogramming.
    (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. **(Feb 08)**
13. (a) Discuss about wilke's microprogrammed control unit
    (b) Explain the organization of control memory **(Nov 07)**

14. i. Discuss about micro instruction sequencing containing the single address field.
    ii. Differentiate between explicit and implicit microinstruction address generation technique. **(Feb 07)**
15. Distinguish between hardwired control and micro programmed control. Explain a micro programmed control unit with the help of a block diagram. **(Feb 07, Nov 02)**

16. i. List sequecing and branching control fields of IBM 3033 micro instructions.
    ii. Discuss the functioning of microsequence of with example. **(Feb 07)**

**UNIT – IV**

1. Explain the computational errors. Why do they occur?. Give some problems where these errors are catastrophic. Also, give some practical examples (algorithms) where error gets
(a) accumulated and
(b) multiplies. [ (JNTU Apr/May 2009)

2. (a) Explain Booth's algorithm with its theoretical basis. [8]
(b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8] (JNTU Apr/May 2009)

3. (a) Multiply 10111 with 10011 using, Booths algorithm. [8]
(b) Explain booths algorithm with its theoretical basis. [8] (JNTU Apr/May 2009)

4. (a) Multiply 10111 with 10011 using, Booths algorithm. [8]
(b) Explain booths algorithm with its theoretical basis. [8] (JNTU Apr/May 2009)

5. Elaborate on different types of registers in a register organization **(Sep 08)**

6. (a) Explain about the machine state register.
(b) Discuss about the sequence of steps that occurs when an interrupt occurs **(Sep 08)**

7. (a) List and describe integer arithmetic and logical instructions of Motorola 88000
(b) Discuss about functioning of Motorola 88000 instruction unit pipeline. **(Sep 08)**

8. (a) List various R3000 pipeline stages. Also explain the function of each.
(b) List and describe all shift and multiply/divide instructions of MIPS R-Series Processors **(May 08)**

9. Elaborate on different types of registers in a register organization **(May 08)**

10. Elaborate on different types of registers in a register organization **(May 08)**

11. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove.
(b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. **(Feb 08)**

12. Draw a flowchart to explain how two IEEE 754 floating point numbers can be added, subtracted and multiplied. Assume single precision numbers. Give example for each **(Feb 08)**

13. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove.
(b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. **(Feb 08)**

14. Write an algorithm to find allowable wieths for a "weighted BCD code". Assume that all weiths are positive numbers. **(Feb 07, Nov 06)**

15. i. Explain how floating point division is done?
ii. Explain the addition binary number in 1's Complement notation. **(Feb 07, Nov 06)**

16. i. Explain about the airthmatic in excess-3 code.
ii. Discuss about normalize floating point. **(Nov 06)**

## UNIT V

1. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. (JNTU Apr/May 2009)
2. (a) "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
(b) A Virtual Memory System has an address space of 8K words and a Memory

space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms: 1) FIFO 2) LRU if the reference string is as follows: 4,2,0,1,2,6,1,4,0,1,0,2,3,5,7. [8+8] (JNTU Apr/May 2009)

3. Explain two-way set associative mapping and four-way set associative mapping techniques with an example for each. [16] (JNTU Apr/May 2009)

4. (a) Compare and contrast FIFO and LRU Cache Replacement Algorithms.
(b) Compare and contrast direct and associative mapping Techniques. (JNTU Apr/May 2009)

5. (a) What are the memory management requirements.
(b) Elaborate on address translation in virtual memories **(Sep 08)**

6. (a) Explain the purpose of address translation. Give a general block diagram of it.
(b) Differentiate between segment table and page table. **(Sep 08)**

7. A block-set-associative Cache consists of a total of 64 blocks divided into four-block sets. The main memory contains 4096 blocks each consisting of 128 words
(a) How many bits are there in main memory address?
(b) How many bits are there in each of the TAG, SET, and WORD fields? **(Sep 08)**

8. (a) Differentiate between single versus two-level caches.
(b) Elaborate on Pentium Cache Organization. **(May 08)**

9. Discuss about address translation with segmentation and paging in the Intel Pentium **(May 08)**

10. Give a block diagram for a 4M×8 memory using 256K×1 memory chips. **(May 08)**

11. (a) Discuss about address translation in paging.
(b) How does page size effects storage utilization and effective memory data transfer rate **(May 08)**

12. (a) Explain how the Bit Cells are organized in a Memory Chip.
(b) Explain the organization of a 1K x 1 Memory with a neat sketch. **(Feb 08)**

13. (a) "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
(b) A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms: 1) FIFO

14. LRU if the reference string is as follows: 4,2,0,1,2,6,1,4,0,1,0,2,3,5,7. **(Feb 08)**

15. Compare and contrast Asynchronous DRAM and Synchronous DRAM. **(Feb 08)**

16. (a) Discuss the principles of associative memory.
(b) Explain the functioning of 4 x 4 bit associative memory array.
(c) Explain the cache with two-way set-associative addressing **(Nov 07)**

17. (a) Explain any three replacement algorithms with examples.
(b) Discuss in detail about set associative mapping in cache memory. **(Nov 07)**

18. (a) Elaborate on functioning of inverted page table structure.

(b) Differentiate between ordinary page table and inverted page table
(c) Why translation-look-aside buffer is used. **(Nov 07)**

19. (a) What is demand paging. Explain it's advantages and disadvantages.
(b) Explain the page table structure. Discuss it's purpose. **(Nov 07)**
20. i. What is deman paging. Explain it's advantage and disadvantage
ii. Explain the page table structure. **(Feb 07)**

21. Write short notes on the following approaches with suitable examples. What are merits and demerits of each.
i. First - fit
ii. Best – fit
iii. Worst – fit **(Feb 07, May 05)**

22. i. Explain the major differences between cache main and main-secondary memory hierachies.
ii. Discuss main features and basic structure of cache. **(Feb 07)**

23. i. Explain the cache execution of a read operation.
ii. Explain look aside system organisation of cache. **(Nov 06)**

24. i. Elaborate about purpose and organization of data on magnetic tape
ii. Differntiate between magnetic disk and magnetic tape.
iii. Discuss the technology used for CD Rom system. **(Nov 06)**

25. i. Define the following term.
a) Hit ratio
b) Miss ratio
ii. What do you mean by cache coherence problem?
iii. Explain how cache memory can be used in pagging. **(Nov 06)**

**UNIT-VI**

**1.** (a) What is Direct Memory Access? Explain the working of DMA.
(b) What are the different kinds of DMA transfers? Explain.
(c) What are the advantages of using DMA transfers? (JNTU Apr/May 2009)

2. Explain the following with respect to serial communication:
(a) Data Communication processor
(b) Modem
(c) Block Transfer
(d) CRC
(e) Full Duplex
(f) Bit oriented protocol. (JNTU Apr/May 2009)
3. What are relative advantages and disadvantages of I/O communication techniques? Explain. [16 (JNTU Apr/May 2009)

4. Write short notes on the following:
(a) RS 232
(b) USB
(c) IEEE 1394. [ (JNTU Apr/May 2009)

5. Discuss about data organization and formatting of magnetic disk in detail **(Sep 08, May 08)**

6. Discuss the major functions and requirements for an I/O module. **(Sep 08)**

7. (a) How would CPU handles multiple devices. Explain with different techniques available
   (b) Discuss the characteristics of Intel 8259A interrupt controller. **(Sep 08, May 08)**

8. Discuss three possible techniques for I/O operations with merits and demerits of each. **(May 08)**

9. (a) Explain about magnetic disk layout
   (b) Elaborate on Winchester disk track format.

10. (a) What are the different types of I/O communication techniques? Give briefnotes.
    (b) In the above techniques, which is the most efficient? Justify your answer **(Feb 08)**

11. (a) Explain bit oriented and character oriented protocols in serial communication.
    (b) What are the different issues behind serial communication? Explain. **(Feb 08)**

12. (a) Differentiate between magnetic-disk and CD-ROM systems.
    (b) Magnetic disks are used as the secondary storage for program and data files in a virtual memory system. Which disk parameter(s) should influence the choice of page size? **(Feb 08)**

13. (a) Differentiate between characteristics of various types of disks
    (b) Elaborate on fixed and movable head disks. **(Nov 07)**

14. (a) Explain about CD-ROM block format.
    (b) What is WORM? Also explain its uses.
    (c) Differentiate between disk layout using constant angular velocity and constant linear velocity **(Nov 07)**

15. (a) Explain how bus arbitration is done in DMA transfer
    (b) Discuss about the generic model of an I/O module. **(Nov 07)**

16. i. Explain about magnetic disk layout.
    ii. Elaborate on Winchester disk track format. **(Feb 07)**

17. Explain about ALU control field of IBM 3033 micor instruction. **(Feb 07)**

18. i. What is data strippting?
    ii. Explain the control commands operation enable be magnetic tape drive controller. **(Feb 07)**

19. i. Differentiate between I/O technique with and without the use of interrupts.
    ii. Explain different type of I/O commands.
    iii. Whatis isolated I/O. Differentiate between memory map and isolated I/O. **(Feb 07)**

20. i. Explain about the magnetic disk principle along with its advantages.
    ii. Discuss the format of a disk address world. **(Nov 06)**

21. i. Discuss about I/O channel architecture.
    ii. Discuss about I/O addressing in 8086.
    iii. Discuss the sailent feature of laser printer. **(Nov 06)**

22. i. Discuss about interrupt structure
    ii. Explain various register in a DMA interface. **(Nov 06)**

23. i. Explain the principal and working of dot matrix printer
    ii. Differentiate between different type of printers. **(Nov 06)**

24. What is Asynchronous data transfer? Explain varous methods of asynchoronous data transfer. **(Nov 06)**

**UNIT-VII**

1. Explain the following with related to the Instruction Pipeline
(a) Pipeline conflicts
(b) Data dependency
(c) Hardware interlocks
(d) Operand forwarding
(e) Delayed load
(f) Pre-fetch target instruction
(g) Branch target buffer
(h) Delayed branch. [8 (JNTU Apr/May 2009)

2. Explain array processors. Explain SIMD array processor organization in detail.
[16] (JNTU Apr/May 2009)

3. Write short notes on the following:
(a) RISC pipeline
(b) Vector processing
(c) Array processors. [5+5+6] (JNTU Apr/May 2009)

4. (a) What is meant by instruction pipeline? Explain four segment Instruction Pipeline.
(b) Give the timing diagram of instruction pipeline. [8 (JNTU Apr/May 2009)

5. (a) Discuss about wilke's microprogrammed control unit
   (b) Explain the organization of control memory **(Sep 08)**

6. (a) Explain about microinstruction format of TI 8800
   (b) Explain about ALU control fields of IBM 3033 microinstruction. **(Sep 08)**

7. (a) Explain the principles and working of dot matrix printers.
   (b) Differentiate between different types of printers. **(Sep 08)**

8. (a) How the address of next microinstruction is known while executing a micro program.
   (b) Discuss about branch control logic in microinstruction sequencing with variable address format. **(Sep 08)**

9. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer **(May 08)**

10. (a) Explain about microinstruction format of TI 8800
    (b) Explain about ALU control fields of IBM 3033 microinstruction. **(May 08)**

11. Discuss about horizontal and vertical instruction formats. Also differentiate between horizontal and vertical instruction formats. **(May 08)**

12. Explain the following with related to the Instruction Pipeline
    (a) Pipeline conflicts
    (b) Data dependency
    (c) Hardware interlocks
    (d) Operand forwarding
    (e) Delayed load
    (f) Pre-fetch target instruction
    (g) Branch target buffer
    (h) Delayed branch. **(Feb 08)**
14. (a) What is pipeline? Explain.
    (b) Explain arithmetic pipeline. **(Feb 08)**
15. (a) What is meant by arithmetic pipeline? Explain.
    (b) Explain pipeline for floating point addition and subtraction. **(Feb 08)**

16. (a) Differentiate between horizontal and vertical micro instructions.
    (b) Discuss about functioning of micro-programmed control unit. **(Nov 07)**

17. (a) Why special handling is required for branch instruction in a pipelined processor. Explain with examples.
    (b) How would you determine the number of pipeline stages in a pipelined processor **(Nov 07)**
18. (a) Differentiate between sequential and pipelined execution of a program
    (b) Explain about instruction execution and hardware organization of a four-stagepipeline **(Nov 07)**
19. Discuss about instruction pipeline **(Feb 07)**

20. i. List the characteristics of super scalar processor and contrast with CICS processor.
    ii. Explain the instruction execution characteristics of RISK processor. **(Feb 07)**

21. Why special handling is require for branch instruction in pipeline processors? Explain with example. **(Nov 06)**
22. Give a summary of arithmetic and logical operation that are defined for the vector architecture. **(Nov 06)**

**UNIT-VIII**

1. (a) Explain serial abitration (Daisy Chain).
(b) Explain prallel abitration. (JNTU Apr/May 2009)
2. (a) Explain multiport memory organization with a neat sketch.
(b) Explain system bus structure for multiprocessors with a neat sketch. [8+8] (JNTU Apr/May 2009)

3. (a) Explain the functioning of omega switching network with a neat sketch. (b) In 8 x 8 omega switching network how many stages are there and in each stage
how many Switches are there.
(c) How many stages and how many Switches in each stage are needed in a n x n
omega sitching network. ( May 09, nov 07, may 01)

4. (a) What is the need of interprocessor synchronization? Explain.
(b) Explain hardwarelock mechanism. (JNTU Apr/May 2009)

5. (a) Explain different types of parallel processors.
   (b) What do you mean by compound instruction? Give examples
   (c) Elaborate on registers of the IBM3090 vector facility. **(Sep 08)**

6. (a) Differentiate between two-stage and four-stage pipelines
   (b) Discuss the demerits of pipelined processing. **(Sep 08)**

7. (a) Explain about directory protocols.
   (b) Draw and explain the state diagram for MESI protocol **(Sep 08)**

8. (a) Give a summary of arithmetic and logical operations that are defined for the vector architecture.
   (b) What is cache coherence problem. Discuss about different cache coherence approches.
   **(May 08)**

9. (a) Explain the following terms.
      i. Read miss
      ii. Read hit
      iii. Write miss
      iv. Write hit
   (b) Discuss different approaches to vector computation **(May 08)**

10. (a) Explain different types of parallel processors.
    (b) What do you mean by compound instruction? Give examples
    (c) Elaborate on registers of the IBM3090 vector facility **(May 08)**

11. (a) Classify and explain different multiprocessors
    (b) Explain the organization of tightly coupled multiprocessor system with a generic block diagram
    **(May 08)**

12. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
    (b) Explain time-shared common bus Organization.
    (c) Explain system bus structure for multiprocessors. **(Feb 08)**

13. What is cache coherence and why is it important in shared memory multiprocessor systems? How can the problem be solved with a snoopy cache controller? **(Nov 07)**

14. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
    (b) Explain time-shared common bus Organization.
    (c) Explain system bus structure for multiprocessors. **(Nov 07)**

15. i. Explain about directory protocol.
    ii. Draw and explain the state diagram MESI protocol. **(Feb 07)**

16. What do you mean by cache coherence problem? **(Feb 07)**

17. i. Differentiate between short and long pieplining. Which is more advantageous?
    ii. Elaborate on depending constratints of pipelining. **(Feb 07)**

18. i. Differentiate between high level and low level parallelism.
    ii. Discuss about Flynns classification of parallel processor system.
    iii. Explain different MIMD interconnection topology. **(Feb 07)**

19. i. Explain different types of parallel processor.
    ii. What do you mean by compound instruction? Give examples.
    iii. Elaborate on register of the IBM 3090 vector facility. **(Nov 06)**